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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,112	03/31/2004	Siva G. Narendra	INTEL-0042	5552
34610 7	590 06/27/2005	EXAMINER		INER
FLESHNER & KIM, LLP			DINKINS, ANTHONY	
	P.O. BOX 221200 CHANTILLY, VA 20153			PAPER NUMBER
CHANTILLY,	VA 20153		2831	

DATE MAILED: 06/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

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		Application No.	Applicant(s)			
Office Action Summary		10/813,112	NARENDRA ET AL.			
		Examiner	Art Unit			
		Anthony Dinkins	2831			
Period fo	The MAILING DATE of this communication app or Reply	ears on the cover sheet with the c	orrespondence address			
THE - External after - If the - If NO - Failu Any I	ORTENED STATUTORY PERIOD FOR REPLY MAILING DATE OF THIS COMMUNICATION. nsions of time may be available under the provisions of 37 CFR 1.13 SIX (6) MONTHS from the mailing date of this communication. period for reply specified above is less than thirty (30) days, a reply period for reply is specified above, the maximum statutory period we re to reply within the set or extended period for reply will, by statute, eply received by the Office later than three months after the mailing and patent term adjustment. See 37 CFR 1.704(b).	within the statutory minimum of thirty (30) days ill apply and will expire SIX (6) MONTHS from cause the application to become ABANDONE	nely filed s will be considered timely. the mailing date of this communication. O (35 U.S.C. § 133).			
Status						
1)🖂	Responsive to communication(s) filed on <u>26 May 2005</u> .					
2a)☐	This action is FINAL . 2b)⊠ This action is non-final.					
3)∐	Since this application is in condition for allowan					
	closed in accordance with the practice under E	x parte Quayle, 1935 C.D. 11, 45	3 O.G. 213.			
Dispositi	on of Claims					
4)🖂	Claim(s) <u>1-30</u> is/are pending in the application.					
	4a) Of the above claim(s) is/are withdrawn from consideration.					
5)⊠	Claim(s) <u>1,3-5,7,8,11,14,15,25 and 27</u> is/are all	lowed.				
	Claim(s) <u>6,9,10,12-14,16 and 28</u> is/are rejected	l.	·			
	Claim(s) <u>17-20,29 and 30</u> is/are objected to.					
8)	Claim(s) are subject to restriction and/or	election requirement.				
Applicati	on Papers					
9)[The specification is objected to by the Examiner	· •				
10)	The drawing(s) filed on is/are: a) acce	epted or b) objected to by the E	Examiner.			
	Applicant may not request that any objection to the o	drawing(s) be held in abeyance. See	e 37 CFR 1.85(a).			
_	Replacement drawing sheet(s) including the correcti					
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.						
Priority u	ınder 35 U.S.C. § 119					
a)[Acknowledgment is made of a claim for foreign All b) Some * c) None of: 1. Certified copies of the priority documents 2. Certified copies of the priority documents 3. Copies of the certified copies of the priority application from the International Bureau see the attached detailed Office action for a list of	s have been received. s have been received in Application ity documents have been received (PCT Rule 17.2(a)).	on No ed in this National Stage			
Attachment	t(s) e of References Cited (PTO-892)	Λ\	(DTO 442)			
2) Notic 3) Inform	e of References Cited (PTO-892) e of Draftsperson's Patent Drawing Review (PTO-948) nation Disclosure Statement(s) (PTO-1449 or PTO/SB/08) r No(s)/Mail Date	4) Interview Summary Paper No(s)/Mail Da 5) Notice of Informal Pa 6) Other:				

Application/Control Number: 10/813,112

Art Unit: 2831

1. Applicant's arguments with respect to claims 1-30 have been considered but are most in view of the new ground(s) of rejection.

2. The indicated allowability of claims 6, 9-10, 12-13, 16, and 28 are withdrawn in view of the rejection shown below and newly discovered reference(s) to Kurabayashi et al. (5,086,373). Rejection of claim 16 is based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 103

- 3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura (6,483,691). Nakamura et al. disclose in Figure 7 an ultracapacitor, comprising a semiconductor substrate (1); N conductive layers (4, 6) on the substrate, and N-1 dielectric layers (5) formed between the conductive layers respectively. Nakamura et al. disclose applicant's claimed invention except for having the N conductive layers as N>2. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the N conductive layers as N>2, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8.

Claim 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura (6,483,691). Nakamura et al. disclose in Figure 7 an ultracapacitor, comprising a semiconductor substrate (1); N conductive layers (4,

6) on the substrate, and N-1 dielectric layers (5) formed between the conductive layers respectively. Nakamura et al. disclose applicant's claimed invention except for having the N conductive layers as N>2 and wherein the N conductive layers include adjacent pairs of conductive layers and wherein the conductive layers in each pair having the same width (re: claim 9) or the conductive layers in each pair being different from the widths of the conductive layers in every other pair (re: claim 10). It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the N conductive layers as N>2 and wherein the N conductive layers include adjacent pairs of conductive layers, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. St. Regis Paper Co. v. Bemis Co., 193 USPQ 8. Furthermore, it would have been an obvious matter of design choice to have the conductive layers in each pair having the same width (re: claim 9) as well as having the conductive layers in each pair being different from the widths of the conductive layers in every other pair (re: claim 10), since such a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. In re Rose, 105 USPQ 237 (CCPA 1955).

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura (6,483,691). Nakamura et al. disclose in Figure 7 an ultracapacitor, comprising a semiconductor substrate (1); N conductive layers (4, 6) on the substrate, and N-1 dielectric layers (5) formed between the conductive layers respectively. Nakamura et al. disclose applicant's claimed invention except for having the N conductive layers as N>2 and wherein the N conductive layers are spaced differently. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the N conductive layers as N>2,

Application/Control Number: 10/813,112

Art Unit: 2831

since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8. Furthermore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have the N conductive layers spaced differently, since it has been held that rearranging parts of an invention involves only routine skill in the art. *In re Japikse*, 86 USPQ 70.

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura (6,483,691). Nakamura et al. disclose in Figure 7 an ultracapacitor. comprising a semiconductor substrate (1); N conductive layers (4, 6) on the substrate, and N-1 dielectric layers (5) formed between the conductive layers respectively. Nakamura et al. disclose applicant's claimed invention except for having the N conductive layers as N>2 and wherein the conductive and dielectric layers form a plurality of capacitors connected in parallel. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the N conductive layers as N>2, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. St. Regis Paper Co. v. Bemis Co., 193 USPQ 8. Furthermore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have the conductive and dielectric layers form a plurality of capacitors connected in parallel, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. St. Regis Paper Co. v. Bemis Co., 193 USPQ 8.

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kurabayashi et al. (5,086,373). Kurabayashi et al. disclose in Figure 1 an ultra first ultracapacitor which also is commonly referred to a double layer capacitor; which could be used in an integrated circuit, col. 1, lines 9-12. Kurabayashi et al.

Application/Control Number: 10/813,112

Art Unit: 2831

disclose in applicant's claimed invention except for having a second ultracapacitor connected in series to the first ultracapacitor. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a second ultracapacitor connected in series to the first ultracapacitor, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8.

Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura (6,483,691). Nakamura et al. disclose in Figure 7 an ultracapacitor, comprising a semiconductor substrate (1); N conductive layers (4, 6) on the substrate, and N-1 dielectric layers (5) formed between the conductive layers respectively. Nakamura et al. disclose applicant's claimed invention except for having the N conductive layers as N>2 and the conductive and dielectric layers store a charge corresponding to a predetermined voltage and form a plurality of capacitors connected in parallel. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the N conductive layers as N>2, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. St. Regis Paper Co. v. Bemis Co., 193 USPQ 8. Furthermore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have a plurality of capacitors connected in parallel which then a charge would be stored at a predetermined voltage since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. St. Regis Paper Co. v. Bemis Co., 193 USPQ 8.

Art Unit: 2831

4. The following is a statement of reasons for the indication of allowable subject matter: Regarding claims 1, 3, 4, 5, 7, 8, 11, 14, 15, 25, and 27 the allowability in combination with the other claimed features is because nowhere in the prior art is there an ultracapacitor having the even numbered ones of the N conductive layers are connected to a first voltage and odd numbered ones of the N conductive layers are set to a second voltage.

Claims 17-20 and 29-30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anthony Dinkins whose telephone number is (571) 272-1972. The examiner can normally be reached on 6:30-3:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean Reichard can be reached on (571) 272-2800 ext.

31. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2831

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Anthony Dinkins Primary Examiner Art Unit 2831

AD.

ANTHONY DINKINS PRIMARY EXAMINER